Abstract of the Disclosure

A semiconductor integrated circuit testing apparatus of the invention comprises a correcting means for correcting input waveform timing of a measuring signal applied to all pins of a semiconductor integrated circuit 5. The correcting means includes: a high-speed clock generating circuit 12 for generating a clock signal; latch circuits 9a, 9b for latching the measuring signal by use of the clock signal from the high-speed clock generating circuit 12; FIFO memories 10a, 10b for storing as data the measuring signal latched by the latch circuits 9a, 9b; and a control circuit 14 for retrieving the data from the FIFO memories 10a, 10b for transfer to a tester.